

Notice of References Cited	Application/Control No. 09/591,270	Applicant(s)/Patent Under Reexamination SHEPARD, KENNETH	
	Examiner Ayal I Sharon	Art Unit 2123	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,023,577	02-2000	Smith et al.	703/14
	B	US-6,141,632	10-2000	Smith et al.	703/14
	C	US-6,281,737	08-2001	Kuang et al.	327/382
	D	US-6,429,684	08-2002	Houston, Theodore W.	326/83
	E	US-6,442,735	08-2002	Joshi et al.	716/4
	F	US-6,490,546	12-2002	Kimmel et al.	703/14
	G	US-6,567,773	05-2003	Rahmat et al.	703/14
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chuang et al., U.S. Patent Application Publication No. US 2003 / 0078763 A1. Filed: April 19, 1999.
	V	Shepard, K.L. et al. "Body-Voltage Estimation in Digital PD-SOI Circuits and Its Application to Static Timing Analysis". 1999 IEEE/ACM Int'l Conf. on CAD. Nov. 7-11, 1999. pp.531-538.
	W	Shepard, K.L. et al. "Harmony: Static Noise Analysis of Deep Submicron Digital Integrated Circuits". 1999 IEEE Transactions on CAD of Integrated Circuits and Systems. August, 1999. pp.1132-1150.
	X	Shepard, K.L. "Design Methodologies for Noise in Digital Integrated Circuits". 1998 ACM/IEEE Design Automation Conference. 1998. pp.94-99.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Notice of References Cited

Application/Control No.

09/591,270

Applicant(s)/Patent Under
Reexamination
SHEPARD, KENNETH

Examiner

Ayal I Sharon

Art Unit

2123

Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-			
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chuang, C.T. "Design Considerations of SOI Digital CMOS VLSI". Proc. 1998 Int'l SOI Conf. Oct. 5-8, 1998. pp.5-8.
	V	Puri, R. and Chuang, C.T. "SOI Digital Circuits: Design Issues". 13th Int'l Conf. on VLSI Design. Jan. 3-7, 2000. pp.474-479.
	W	Sinitsky, D. et al. "Simulation of SOI Devices and Circuits using BSIM3SOI". IEEE Electron Device Letters. Sept. 1998. pp.323-325.
	X	Tu, R. "Simulation of Floating Body Effect in SOI Circuits Using BSIM3SOI". 1997 Int'l Symposium on VLSI Technology, Systems, and Applications, 1997. June 3-5, 1997. pp.339-342.

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.